Art Unit: 2813

Attorney Docket No.: 740756-2101

Page 2

Bros

not formed at the side of a drain region 208 of the n-channel TFT, and this becomes a structure that prevents reduction of the operational frequency due to a parasitic capacity.--

IN THE DRAWINGS:

Corrections have been made to Figs. 7A, 8C, 10, 12A, 12C, 24A and 26C with a Request for Approval of Drawing Corrections filed concurrently herewith.

IN THE CLAIMS:

Please cancel claims 45-80 without prejudice or disclaimer of the subject matter contained therein.

Please amend claims 1, 2, 9-11, 18-20, 27, and 36 as follows. Claims 1, 2, 9-11, 18-20, 27 and 36 are presented below in their amended form. The amendments to the above-noted claims are outlined in an Attachment to the Amendment using the conventional indication method of bracketing and underlining.

- 1. (Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:
- a) said driver circuit includes:
 - a first thin film transistor comprising:
- a channel forming region and a third impurity region having n-type conductivity, formed on the inside of a gate electrode; and
- a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode; and
 - a fifth thin film transistor comprising:
- a channel forming region, and a fifth impurity region having p-type conductivity which forms a source region or a drain region; and
- b) said pixel section comprises!
 - a fourth film transistor comprising:
 - a channel forming region formed on the inside of a gate electrode; and

Jube, 0

Application No.: 09/502,675 Attorney Docket No.: 740756-2101 Page 3

Art Unit: 2813

a fourth impurity region having the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode.

A semiconductor device according to claim 1, wherein: 2. (Amended)

an impurity element having the n-type conductivity is included in the third impurity region and in the fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

9. (Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:

a) said driver circuit comprises:

a first thin film transistor comprising:

a channel forming region and a third impurity region having n-type conductivity, formed on the inside of d gate electrode; and

a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode;

a second thin film transistor comprising:

a channel forming region and a third impurity region having the n-type conductivity, formed on the inside of a gate electrode; and

a second impurity region having the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region, and a fifth impurity region having p-type conductivity which forms a source region or a drain region; and b) said pixel section comprises:

NVA210864.1

Art Unit: 2813

Attorney Docket No.: 740756-2101

Page 4

a fourth thin film transistor having:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode.

10. (Amended) A semiconductor device according to claim 2, wherein:

an impurity element having the n-type conductivity is included in the third impurity region and in the fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

11. (Amended) A semiconductor device according to claim 9, wherein:

an impurity element having the n-type conductivity is included in the second impurity region and in the third impurity region; and

a concentration of the impurity element included in said second impurity region is the same as a concentration of the impurity element included in said third impurity region.

18. (Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate wherein:

a) said driver circuit comprises:

a third thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a second impurity region having n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode; and

a fifth thin film transistor comprising:

Brown of the second

Art Unit: 2813

Attorney Docket No.: 740756-2101

Page 5

a channel forming region, and a fifth impurity region having p-type conductivity which forms a source region or a drain region; and

b) said pixel section comprises:

- a fourth thin film transistor comprising:
- a channel forming region formed on the inside of a gate electrode; and
- a fourth impurity region having the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode.

Brall

- 19. (Amended) A semiconductor device according to claim 18, wherein: a length of said second impurity region is 0.5 to 3.0 μm.
- 20. (Amended) A semiconductor device according to claim 18, wherein: said third and fifth thin film transistor constitute a sampling circuit.
- 27. (Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:
- a) said driver circuit comprises:
 - a first thin film transistor comprising:
- a channel forming region and a third impurity region having n-type conductivity, formed on the inside of a gate electrode; and
- a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode;

wherein said first thin film transistor constitutes a shift register circuit, and

a second thin film transistor comprising:

a channel forming region and the third impurity region having the n-type conductivity, formed on the inside of a gate electrode; and

Art Unit: 2813

Attorney Docket No.: 740756-2101

Page 6

a second impurity region having the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode;

wherein said second thin film transistor constitutes a sampling circuit, and b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode.

- 36. (Amended) A semiconductor device having a panel comprising a pixel section and a driver circuit formed over a substrate, wherein:
- a) said pixel section comprises a thin film transistor comprising:
 - a semiconductor layer formed over an insulating surface of said substrate;
- a gate insulating film on said semiconductor layer and a gate electrode over said gate insulating film;
 - a channel forming region formed in said semiconductor layer;
 - a source region and a drain region formed in said semiconductor layer; and
- a lightly doped drain (LDD) region, formed in said semiconductor layer so as not to be overlapped with said gate electrode, and
- b) said driver circuit comprises:
 - a first thin film transistor comprising:
 - a first semiconductor layer formed over an insulating surface of said substrate;
- a gate insulating film on said first semiconductor layer and a first gate electrode over said gate insulating film;
 - a first channel forming region formed in said semiconductor layer;
 - a first source region and a first drain region formed in said first semiconductor layer; and

